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EXAMINER	
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2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,773	BISHOP ET AL.	
	Examiner	Art Unit	
	Nithya Janakiraman	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the submission filed on 6/26/2007. Claims 1-8 and 10-36 are presented for examination.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/27/2007 has been entered.

Claim Objections

2. Claim 34 is objected to because of the following informality: the Examiner recommends amending the phrase "means for permitted" to "means for permitting".

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 26-31 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. Claim 26 recites "a first software program" which is rejected as being directed towards nonstatutory subject matter in the form of software *per se*. Claims 27-31 are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 5-8, 10, 11, 13-19, 21-24, 26-30, 32-35 are rejected under 35 U.S.C. 102(b) as being anticipated by "Operating Systems Concepts", Fifth Edition by Silberschatz and Galvin (hereinafter OSC).

6. Regarding claim 1, OSC discloses:

A method comprising:

emulating an operation of a client (Section 3.6, "virtual machines", virtual machines can emulate real machines, or clients which are shown in Section 3.3.5, "The source of the communication, known as the client and the receiving daemon, knows as a server, then exchange message by read message and write message system calls.");

comparing a first identifier (Figure 8.16, "page number", **p**) in a pointer (Figure 8.16, "logical address") used by the emulated operation (Section 3.6, operation of a virtual machine) with a second identifier included in a table entry (Figure 8.16, **p,** "Translation Look Aside Buffers",), wherein an address to a contiguous portion of emulated memory (Physical memory is being

"emulated" by using the logical address because the CPU operates as though the data is at **p** and **d** when in reality it is located at **f** and **d**) is included in both the pointer and the table entry (Chapter 8, page 263, "...translation look aside buffers (TLBs). A set of associative registers is built of especially high-speed memory. Each register consists of two parts: a key and a value. When the associative registers are presented with an item, it is compared with all keys simultaneously. If the item is found, the corresponding value field is output...Associative registers are used with page tables in the following way. The associative registers contain only a few of the page-table entries. When a logical address is generated by the CPU, its page number is presented to a set of associative registers that contain page numbers and their corresponding frame numbers. If the page number is found in the associative registers, it frame number is immediately available is used to access memory");

and

accessing the contiguous portion of emulated memory with the emulated operation-only-when the first and second identifiers are the same (Figure 8.16, "physical address" to "physical memory").

7. Regarding claim 2, OSC discloses:

The method as defined in Claim 1, wherein:

the table entry is in a table that includes a plurality of said table entries (Figure 8.12, "page table");

each said table entry references an address of one said contiguous portion of the emulated memory (page 257, "page table contains base address of each page in physical memory");

the pointer is one of a plurality of said pointers (Figure 8.12); and

each said pointer includes:

the address of a respective said contiguous portion of the emulated memory (this is the definition of a pointer); and

said identifier corresponding to the respective said contiguous portion of the emulated memory (Figure 8.12).

8. Regarding claim 3, OSC discloses:

The method as defined in Claim 1, wherein

the accessing further comprises identically changing the identifier in both of the corresponding pointer to contiguous portion of emulated memory and the corresponding table entry when the permitted access is not a read or a write operation (Figure 8.8, Memory Allocation).

9. Regarding claim 5, OSC discloses:

A computer-readable medium comprising instructions that, when executed by a computer, performs the method of claim 1 (inherently necessary to perform the method of claim 1).

10. Regarding claim 6, OSC discloses:

A method comprising:

making a call to a memory manager for an emulated memory access operation (Physical memory is being "emulated" by using the logical address because the CPU operates as though the data is at **p** and **d** when in reality it is located at **f** and **d**) to an allocated contiguous portion of emulated

memory, wherein a generation count has been assigned to (Figure 8.12):

a plurality of table entries corresponding to a respective plurality of said allocated contiguous portions of emulated memory (Figure 8.12, "page table"), and

a plurality of pointers each including an address to a respective said allocated contiguous portion of emulated memory (this is the definition of a pointer);

comparing the generation count:

in the pointer including the address to the allocated contiguous portion of emulated memory (Figure 8.16, "logical address"); and

in the table entry corresponding to the allocated contiguous portion of emulated memory (Figure 8.16, "page table");

if the respective said generation counts in the comparison do not match,

then outputting a diagnostic (page 256, "valid-invalid bit"); and

if the respective said generation counts in the comparison match, removing the generation count from the pointer specified by the memory manager for the emulated memory access operation (Physical memory is being "emulated" by using the logical address because the CPU operates as though the data is at **p** and **d** when in reality it is located at **f** and **d**) during the performing of the emulated memory access operation for which the memory manager was called (Chapter 8, page 263, "...translation look aside buffers (TLBs). A set of associative registers is built of especially high-speed memory. Each register consists of two parts: a key and a value. When the associative registers are presented with an item, it is compared with all keys simultaneously. If the item is found, the corresponding value field is output...Associative registers are used with page tables in the following way. The associative registers contain only a few of the page-table entries. When

a logical address is generated by the CPU, its page number is presented to a set of associative registers that contain page numbers and their corresponding frame numbers. If the page number is found in the associative registers, it frame number is immediately available is used to access memory").

11. Regarding claim 7, OSC discloses:

The method as defined in Claim 6, further comprising:

performing the emulated memory access operation for which the memory manager was called when there is a match of the respective said generation counts (page 265, "sets the bit for each page to allow or disallow accesses to that page");

and preventing the performance of the emulated memory access operation for which the memory manager was called when the respective said generation counts of the comparison do not match (page 265, "sets the bit for each page to allow or disallow accesses to that page").

12. Regarding claim 8, OSC discloses:

The method as defined in Claim 7, further comprising, when there is a match and the emulated memory access operation is not a read or a write operation, incrementing the generation count in both:

the pointer including the address to the allocated contiguous portion of emulated memory (this is the definition of a pointer); and

the table entry corresponding to the allocated contiguous portion of emulated memory (Figure 8.12).

13. Regarding claim 10, OSC discloses:

The method as defined in Claim 6, wherein the emulated memory access operation is selected from the group consisting of:

a read operation (page 239);

a write operation (page 239);

a reallocation operation (Section 8.4, "Contiguous Allocation"); and

an operation to free one or more of said allocated contiguous portions of emulated memory (Figure 8.8).

14. Regarding claim 11, OSC discloses:

The method as defined in Claim 6, further comprising, prior to the making of the call:

making a call to the memory manager for to allocate a contiguous portion of emulated memory (page 251, "The operating system keeps a table indicating which parts of memory are available and which are occupied. Initially, all memory is available for user processes and is considered as one large block of available memory, a hole. When a process arrives and needs memory, we search for a hole large enough for this process. If we find one, we allocate only as much memory as is needed keeping the rest available to satisfy future requests");

receiving one said pointer from the memory manager that includes the address of the allocated contiguous portion of emulated memory (Figure 8.12 depicts a literal pointer to the "page table");

performing the allocation of the contiguous portion of emulated memory (Figure 8.8, memory is

being allocated and reallocated depending on available space);

and inserting the generation count:

in the:

the pointer containing including the address to the one said allocated contiguous portion of emulated memory (this is the definition of a pointer); and

the plurality of table entries corresponding to the one said allocated contiguous portion of emulated memory (Physical memory is being "emulated" by using the logical address because the CPU operates as though the data is at **p** and **d** when in reality it is located at **f** and **d**; Figure 8.12, the page table contains a plurality of entries).

15. Regarding claim 13, OSC discloses:

A computer-readable medium comprising instructions that, when executed by a computer, performs the method of Claim 12 (inherently necessary to perform the method of claim 12).

16. Regarding claim 14, OSC discloses:

In a first computing device executing a first application for the emulation of a second computing device executing a second application (Figure 8.12), a method comprising:

making a call from the second application to a memory manager for an emulated memory access operation to an allocated contiguous portion of emulated memory used by the second application and including a plurality of said allocated contiguous portions (Figure 8.12, "physical memory"), wherein:

a generation count is in a plurality of table entries corresponding to a respective plurality of said

allocated contiguous portions of emulated memory (Figure 8.12, "page table");

a generation count is in a plurality of pointers each including an address to a respective said allocated contiguous portion of emulated memory (this is the definition of a pointer);

for the emulated memory access operation, the memory manager uses the address in the pointer that corresponds to the allocated contiguous portion in emulated memory after removal of the generation count from the pointer (Figure 8.12, "physical address"); and

prior to performing the emulated memory access operation to the allocated contiguous portion of emulated memory:

comparing the generation count:

in the pointer including the address of the allocated contiguous portion of the emulated memory (Figure 8.12, 'p'); and

in the table entry corresponding to the allocated contiguous portion of the emulated memory (Figure 8.12, 'f');

outputting a diagnostic when the respective said generation counts of the comparison do not match (page 265, "valid-invalid bit").

17. Regarding claim 15, OSC discloses:

The method as defined in Claim 14, further comprising:

performing the emulated memory access operation for which the memory manager was called when there is a match of the respective said generation counts (Section 8.5.1, "Basic Method"); and

preventing the performance of the emulated memory access operation for which the memory

manager was called when the respective said generation counts of the comparison do not match (Section 8.5.1, "Basic Method").

18. Regarding claim 16, OSC discloses:

The method as defined in Claim 15 further comprising, when there is a match of the respective said generation counts and the emulated memory access operation is not a read operation or a write operation, incrementing the generation count in both (Page 256, "...when compaction is possible..."; Figure 8.8, "Memory Allocation"):

the pointer including the address to the allocated contiguous portion of emulated memory (this is the definition of a pointer); and

the table entry corresponding to the allocated contiguous portion of emulated memory (Figure 8.12, 'f').

19. Regarding claim 17, OSC discloses:

The method as defined in Claim 14, further comprising,

when:

the comparison finds that there is a match of the respective said generation counts (Figure 8.12, 'p', 'f'); and

the emulated memory access operation is neither a read operation nor a write operation:

performing the emulated memory access operation for which the memory manager was called and during which the generation count is removed from the pointer used by the memory manager (Figure 8.8, "Memory Allocation").

20. Regarding claim 18, OSC discloses:

The method as defined in Claim 14, wherein the emulated memory access operation is selected from the group consisting of:

a read operation (page 239);

a write operation (page 239);

a reallocation operation (Section 8.4, "Contiguous Allocation"); and

an operation to free one or more of said allocated contiguous portions of emulated memory (Figure 8.8).

21. Regarding claim 19, OSC discloses:

The method as defined in Claim 14, further comprising, prior to the making of the call by the second application to the memory manager for the emulated memory access operation:

making a call by the second application to the memory manager for an allocation of said allocated contiguous portion of emulated memory (Figure 8.8);

receiving one said pointer from the memory manager that contains includes an address to said allocated contiguous portion of emulated memory (this is the definition of a pointer);

performing an allocation of said allocated contiguous portions of emulated memory (Figure 8.8); and

incrementing the generation count in both:

the pointer including the address to said allocated contiguous portion of emulated memory (Figure 8.16); and

the table entry corresponding to said allocated contiguous portion of emulated memory (Figure 8.16, "page table").

22. Regarding claim 21, OSC discloses:

A computer-readable medium comprising instructions that, when executed by a computer, performs the method of Claim 14 (inherently necessary to perform the method of claim 14).

23. Regarding claim 22, OSC discloses:

A computer-readable medium including instructions for execution by a computer, wherein the instructions comprise:

first logic calling for an emulated memory access operation with respect to a first of a contiguous portion of an emulated memory (Figure 8.16, "physical memory") for which there is:

a corresponding table entry in a table having a plurality of said table entries that map to respective other said portions of the emulated memory (Figure 8.16, "page table"),

wherein each said table entry includes an identifier; and

a corresponding pointer to a plurality of pointers each including an identifier and an address to a respective said contiguous portion of the emulated memory (Figure 8.16, "physical address");

second logic, in response to the first logic, such that, if the identifier in the table entry corresponding to the first said contiguous portion is the same as the identifier in the pointer corresponding to the first said portion (Figure 8.16), then:

the emulated memory access operation is performed with respect to the first said contiguous portion of the emulated memory (Figure 8.16, "physical memory"); and

when the emulated memory access operation is neither a read operation nor a write operation, the identifier is identically changed in both (Figure 8.8, "Memory Allocation"):

the table entry corresponding to the first said portion (Figure 8.16); and

the pointer corresponding to the first said portion (Figure 8.16, "physical address");

third logic, when the identifier in the table entry corresponding to the first said contiguous portion is different from the identifier in the pointer corresponding to the first said portion, calling for a diagnostic to be output (page 256, "valid-invalid bit").

24. Regarding claim 23, OSC discloses:

The computer-readable medium as defined in Claim 22, wherein the emulated memory access operation is selected from the group consisting of:

a read operation (page 239);

a write operation (page 239);

a reallocation operation (Section 8.4, "Contiguous Allocation"); and

an operation to free one or more of said portions of the emulated memory (Figure 8.8).

25. Regarding claim 24, OSC discloses:

The computer-readable medium as defined in Claim 22, wherein the performance of the memory operation further comprises removing the identifier from the pointer corresponding to the first said contiguous portion during the performance of the memory operation (Figure 8.16).

26. Regarding claim 26, OSC discloses:

A first software program which, when executed by a computing device, emulates the execution of a second software program using emulated memory, the first software program comprising instructions that permit the second software program to perform an emulated memory access operation on a previously allocated contiguous portion of the emulated memory only when a pointer and a table entry both include the same identifier (Chapter 8, page 263, "...translation look aside buffers (TLBs). A set of associative registers is built of especially high-speed memory. Each register consists of two parts: a key and a value. When the associative registers are presented with an item, it is compared with all keys simultaneously. If the item is found, the corresponding value field is output...Associative registers are used with page tables in the following way. The associative registers contain only a few of the page-table entries. When a logical address is generated by the CPU, its page number is presented to a set of associative registers that contain page numbers and their corresponding frame numbers. If the page number is found in the associative registers, it frame number is immediately available is used to access memory"), wherein:

the pointer also includes an address to the previously allocated contiguous portion which is useable to access the previously allocated contiguous portion after removal of the identifier (Figure 8.16, "physical memory"); and

the table entry maps to the previously allocated contiguous portion (Figure 8.16, "page table").

27. Regarding claim 27, OSC discloses:

The first software program as defined in Claim 26, wherein:

the table entry is one of a plurality of said table entries that map to a respective plurality of said

portions of the emulated memory (Figure 8.16, "page table"); and

the pointer is one of a plurality of said pointers that each include:

the address to a respective said contiguous portion of the emulated memory (this is the definition of a pointer); and

one said identifier corresponding to the respective said contiguous portion of the emulated memory (Figure 8.16, "physical address").

28. Regarding claim 28, OSC discloses:

The first software program as defined in Claim 26, wherein the performance of the emulated memory access operation on the contiguous portion of the emulated memory further comprises:

removing the identifier from the corresponding pointer when it is processed by the execution of the second software program (Figure 8.16); and

when the emulated memory access operation is neither a read operation not a write operation, identically changing the identifier with the first software program in both of the corresponding pointer and table entry after the execution of the second software program has performed the emulated memory access operation on the contiguous portion of the emulated memory (Figure 8.8, "Memory Allocation").

29. Regarding claim 29, OSC discloses:

The first software program as defined in Claim 27, wherein the instructions further comprise removing the identifier from each said pointer prior to its use by the second software program (Figure 8.8, "Memory Allocation").

30. Regarding claim 30, OSC discloses:

The first software program as defined in Claim 27, wherein the instructions further comprise use of the table entries and identifiers with the first software program but not by the second software program (Figure 8.8, "Memory Allocation").

31. Regarding claim 32, OSC discloses:

A computer-readable medium including instructions for execution by a computer, wherein the instructions comprise:

means for emulating an operation of a client (Section 3.3.5, "The source of the communication, known as the client and the receiving daemon, knows as a server, then exchange message by read message and write message system calls") as the client executes an application (page 259, the logical address emulates the physical address); and

means for outputting a diagnostic when:

the emulated operation attempts to access a previously allocated contiguous portion of emulated memory using a pointer including an identifier, wherein the pointer is configured to access the previously allocated contiguous portion of the emulated memory upon removal of the identifier (page 256, "valid-invalid identifier"); and

a table entry used to manage the emulated memory does not include the same identifier as the identifier in the pointer, wherein an address to the previously allocated contiguous portion is included in both the pointer and the table entry (Chapter 8, page 263, "...translation look aside buffers (TLBs). A set of associative registers is built of especially high-speed memory. Each

register consists of two parts: a key and a value. When the associative registers are presented with an item, it is compared with all keys simultaneously. If the item is found, the corresponding value field is output...Associative registers are used with page tables in the following way. The associative registers contain only a few of the page-table entries. When a logical address is generated by the CPU, its page number is presented to a set of associative registers that contain page numbers and their corresponding frame numbers. If the page number is found in the associative registers, it frame number is immediately available is used to access memory").

32. Regarding claim 33, OSC discloses:

The computer-readable medium as defined in Claim 32, wherein:

the table entry is in a table that includes a plurality of said table entries (Figure 8.16, "page table");

each said table entry references an address of one said previously allocated contiguous portion of the emulated memory (Figure 8.16, 'f');

the pointer is one of a plurality of said pointers (Figure 8.16, "page table"); and

each said pointer includes:

the address to a respective said previously allocated contiguous portion of the emulated memory (this is the definition of a pointer); and

one said identifier corresponding to the respective said previously allocated contiguous portion of the emulated memory (Figure 8.16, 'f').

33. Regarding claim 34, OSC discloses:

The computer-readable medium as defined in Claim 32, further comprising means for permitted the attempted access by the emulated operation to the previously allocated contiguous portion of emulated memory, wherein during prior to said access:

the identifier is removed from the corresponding pointer to the contiguous portion of emulated memory (Figure 8.8, "Memory Allocation"); and

when the permitted access is not a read or a write operation, the identifier in both of the corresponding pointer to contiguous portion of emulated memory and the corresponding table entry is identically changed (Figure 8.8, "Memory Allocation").

34. Regarding claim 35, OSC discloses:

The computer-readable medium as defined in Claim 34, further comprising:

means, prior to an allocation of the previously allocated contiguous portion of emulated memory, for making a call to a memory manager for an allocation of the previously allocated contiguous portion of emulated memory (Figure 8.8);

means for receiving the pointer from the memory manager that includes the address to the previously allocated contiguous portion of emulated memory (Figure 8.12);

means for performing the allocation of the previously allocated contiguous portion of emulated memory (8.12, "physical memory");

means for inserting the generation count in the table entry (Figure 8.12, "page table"); and

means for copying the generation count from the table entry to the pointer (Figure 8.12, 'f').

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 4, 12, 20, 25, 31, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Operating System Concepts.

36. Operating System Concepts discloses the concepts of memory allocation and paging.

37. However, OSC does not explicitly disclose these concepts being conducted on such clients as a personal computer, workstation, server, set top box, video game console, Personal Digital Assistant, cellular telephone, or handheld computing device.

38. Official Notice is being taken that each one of these devices is capable of being a client, and was well know at the time the invention was made in the analogous art of client-server technology.

39. At the time the invention was made it would have been obvious to a person of ordinary skill in the art to use the recited devices as clients as specified in claims 4, 12, 20, 25, 31, and 36.

40. The motivation to do so would have been to make the method compatible with a plurality of client platforms, which have a variety of benefits including an expanded market, a larger customer base, etc. Section 1.5 details various computing systems.

41. Therefore, it would have been obvious to modify Operating Systems Concepts to include such clients as a personal computer, workstation, server, set top box, video game console, Personal Digital Assistant, cellular telephone, or handheld computing device.

Response to Arguments- 35 U.S.C §101

42. Applicant's arguments, see page 23, filed 6/26/2007, with respect to clams 1-5 have been fully considered and are persuasive. The rejections of claims 1-5 have been withdrawn.

Response to Arguments- 35 U.S.C §103

43. Applicant's arguments with respect to claims 1-8 and 10-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nithya Janakiraman whose telephone number is 571-270-1003. The examiner can normally be reached on Monday-Thursday, 8:00am-5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571)272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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